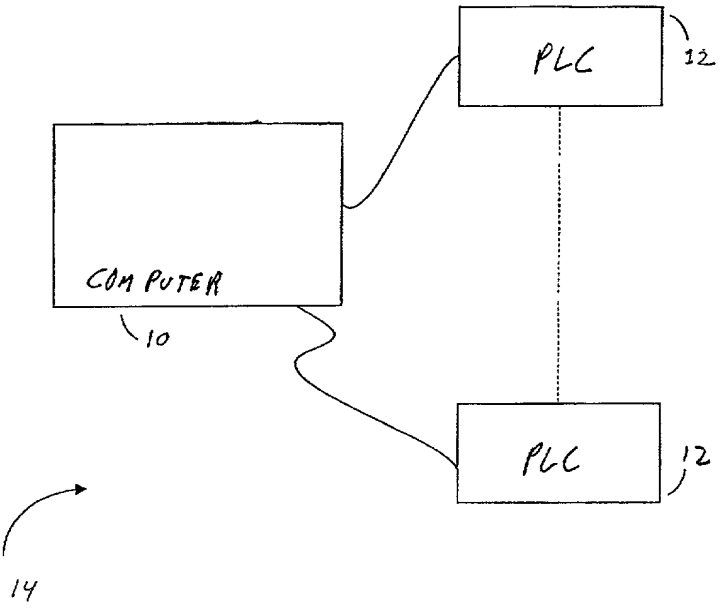
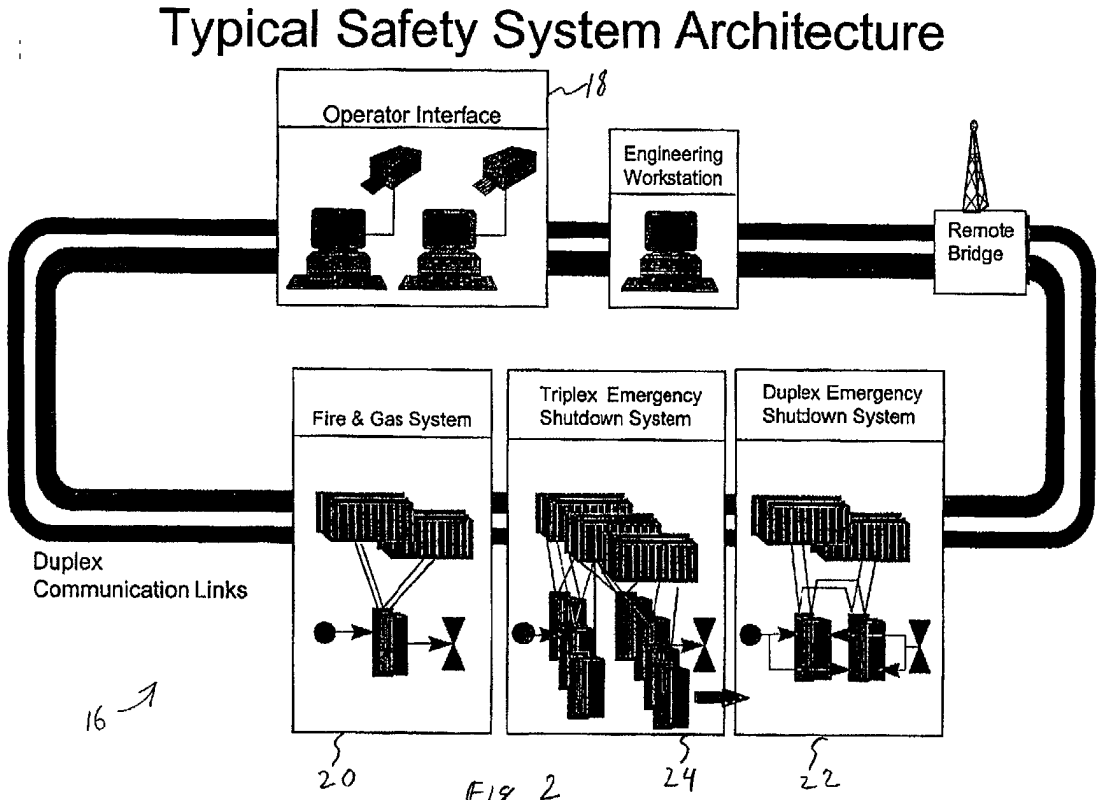


FIG. 1


Typical Safety System Architecture
Operator Interface
18
Engineering Workstation
Remote Bridge
Fire & Gas System
Triplex Emergency Shutdown System
Duplex Emergency Shutdown System
Duplex Communication Links
16
20
24
22

2/9

Fig 2

Defining a formal methodology for specification of functional requirements for a target system based upon Cause and Effect notation and function blocks. ~32

30

Employing a computer-aided specification tool-set to support capture and validation of functional requirements. ~34

Employing a software module to directly execute Cause and Effect application logic. ~36

Fig 3

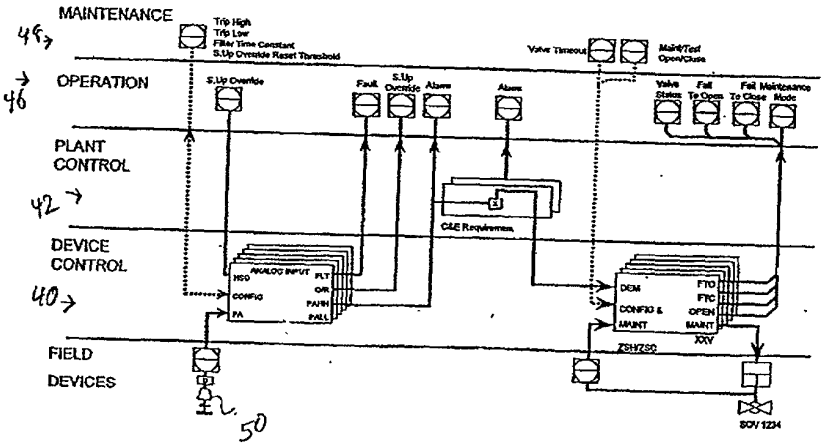


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Fig 4

54

Symbol	Name	Description
X_n	OR	Input term is or'ed into Gate n
$\bar{X}_n$	INV OR	Input term is inverted and or'ed into Gate N
$\&_n$	AND	Input term is and'ed into Gate n
$\bar{\&}_n$	INV AND	Input term is inverted and and'ed into Gate n
E_n	ENABLE	Input term is or'ed with other enables. These terms are used to enable or'ed/and'ed terms of Gate n. If no enable terms are defined then gate is enabled.
$\bar{E}_n$	INV ENABLE	Input term is inverted and or'ed with other enables. These terms are used to enable or'ed/and'ed terms of Gate n. If no enable terms are defined then gate is enabled.
$T(NN)_n$	ONTIMER	Input term is subject to on delay of NN seconds Timer output is or'ed into group n.
$\bar{T}(NN)_n$	INV ONTIMER	Input term is inverted and subject to on delay of NN seconds. Timer output is or'ed into group n.
R	RESET	Input term resets latch. Latch set term has priority. If no reset terms are defined for a gate then gate is non-latching.
$\bar{R}$	INV RESET	Input term resets latch when false. Latch set term has priority. If no reset terms are defined for a gate then gate is non-latching

CAUSE & EFFECT INSTRUCTION SET SUMMARY

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Fig 5

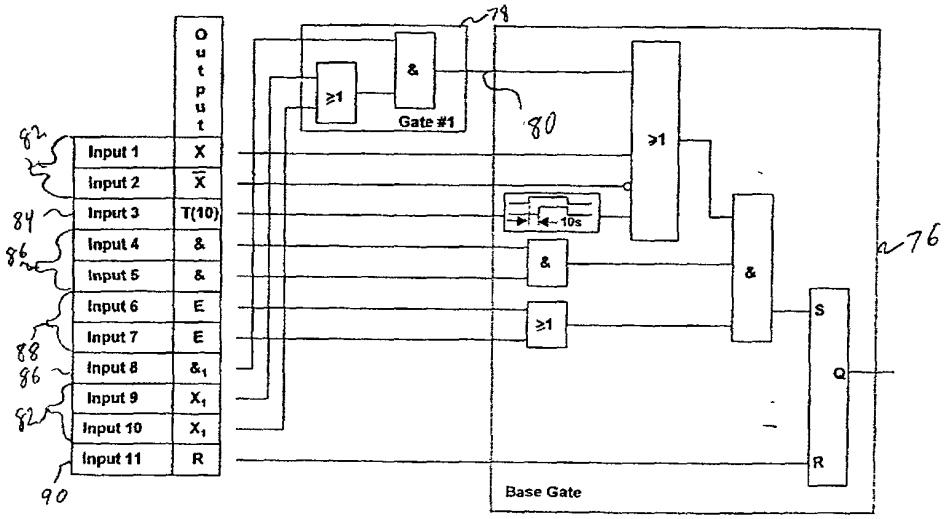


Fig 6

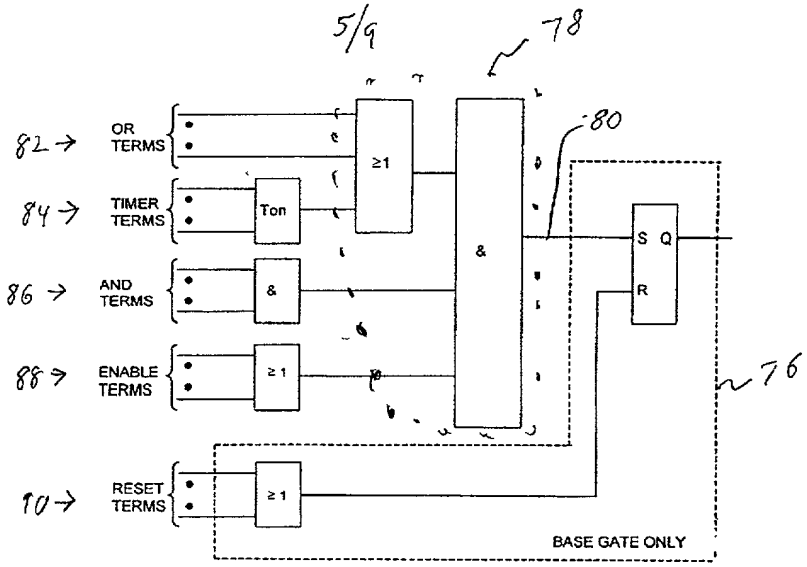

78
80
82
OR TERMS
84
TIMER TERMS
Ton
86
AND TERMS
88
ENABLE TERMS
90
RESET TERMS
≥1
&
S Q
R
76
BASE GATE ONLY

Fig. 7

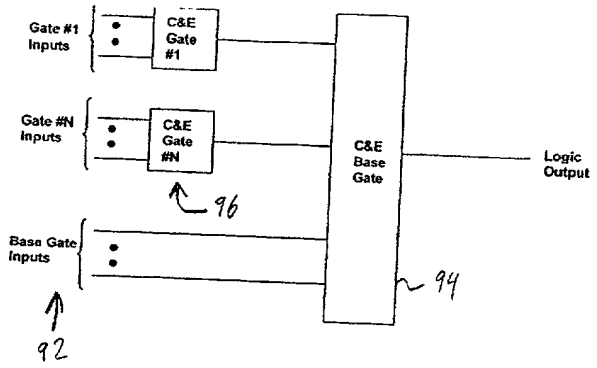

Gate #1 Inputs
C&E Gate #1
Gate #N Inputs
C&E Gate #N
96
Base Gate Inputs
92
C&E Base Gate
Logic Output
94

Fig 8

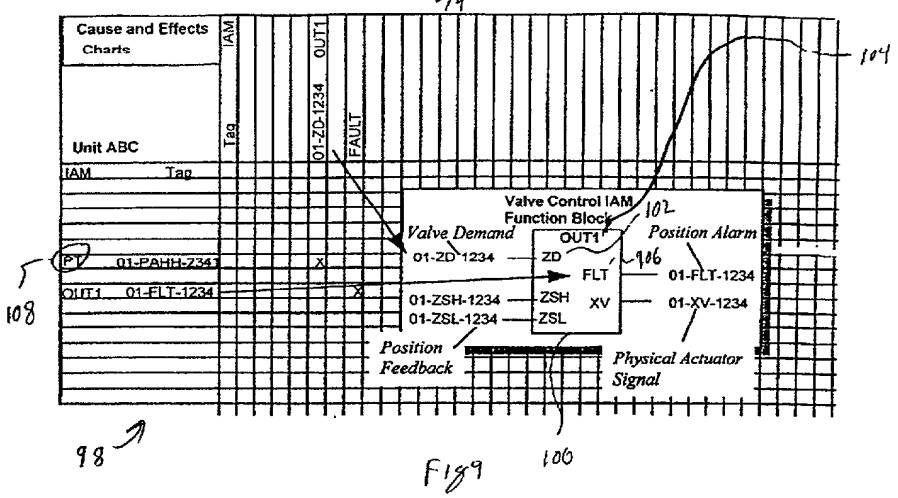


Fig 9

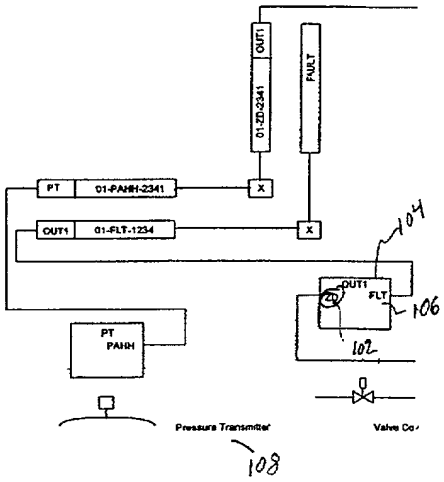


FIGURE 10

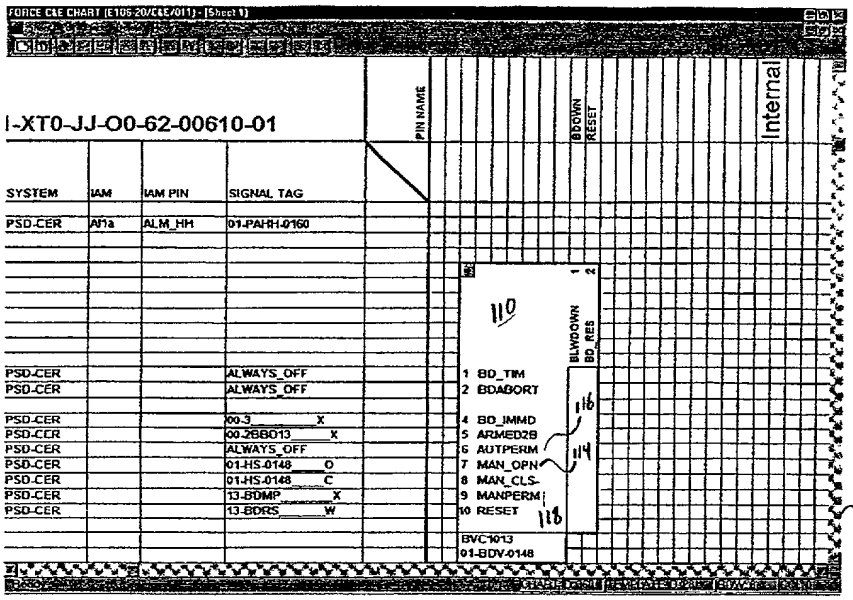

FORCE C&E CHART (E105-20/C&E/011) - [Sheet 1]
I-XT0-JJ-O0-62-00610-01
PIN NAME
BDDWN
RESET
Internal
SYSTEM
IAM
IAM PIN
SIGNAL TAG
PSD-CER
AM1a
ALM_HH
01-PAHH-0160
PSD-CER
ALWAYS_OFF
PSD-CER
ALWAYS_OFF
PSD-CER
00-3 X
PSD-CER
00-26BO13 X
PSD-CER
ALWAYS_OFF
PSD-CER
01-HS-0148 O
PSD-CER
01-HS-0148 C
PSD-CER
13-BDMP X
PSD-CER
13-BDRS W
110
BLWDOWN
BD_RES
1 BD_TIM
2 BDABORT
4 BD_IMMD
5 ARMED28
6 AUTPERM
7 MAN_OPN
8 MAN_CLS
9 MANPERM
10 RESET
116
114
118
BVC1013
01-BDV-0148
112
120

FIGURE 11

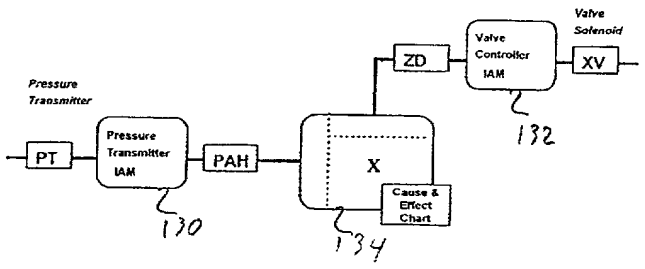


FIGURE 12

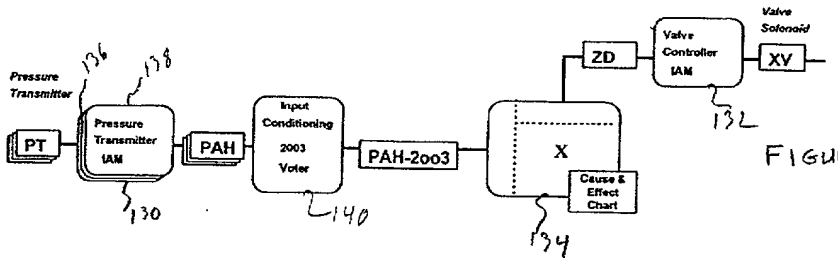
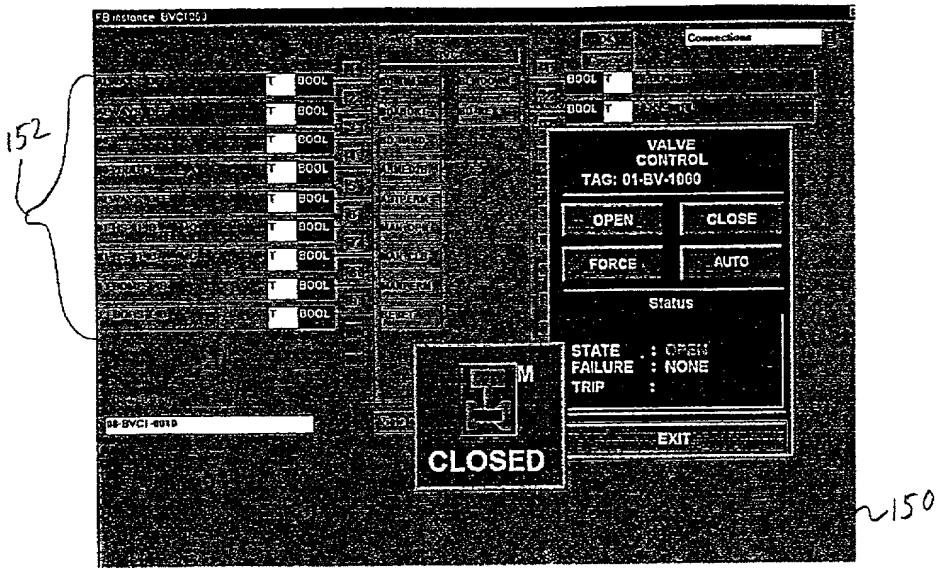


FIGURE 13



FUNCTION BLOCK LOGIC TEMPLATE AND ASSOCIATED HMI ELEMENTS

Figure 14